International Journal of Electronics Communication and Computer Engineering
Volume 4, Issue 1, ISSN (Online): 2249–071X, ISSN (Print): 2278–4209

Area Efficient Single Phase Clock Divider

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***Abstract* — In this paper the prescaler circuit which is used by frequency synthesizers of Bluetooth, zigbee and WLAN is proposed with multi modulus 32/33/47/48 prescaler, ultra low power 2/3 prescaler and integrated P-counter and S-counter. This proposed prescaler can divide the frequency in three bands 0f 2.4-2.484GHz, 5.15-5.35GHz and 5.725-5.825GHz with a resolution selectable from 1-25MHz.The Area and power consumed by the 2/3 prescaler circuit is minimized.**

***Keywords* — DFF, Frequency Synthesizer, U-TSPC, Wireless LAN (WLAN), True Single Phase Clock (TSPC).**

I. INTRODUCTION

Wireless LAN (WLAN) in the multigigahertz bands, such as HiperLAN II and IEEE 802.11a/b/g, are the leading standards for high-rate data transmissions, and standards like IEEE 802.15.4 are recognized for low-rate data transmissions. The demand for lower cost, lower power, and multiband RF circuits increased in conjunction with need of higher level of integration. The frequency synthesizer, usually implemented by a phase-locked loop (PLL) is one of the power-hungry blocks in the RF front-end, and the first-stage frequency divider consumes a large portion of power in a frequency synthesizer. The integrated synthesizers for WLAN applications at 5GHz reported in [2] and [4] consume up to 25mW in CMOS realizations.

The frequency synthesizer reported in [5] uses an E-TSPC prescaler as the first-stage divider, but the divider consumes around 6.25mW. Most of the IEEE 802.11a/b/g frequency synthesizers employ SCL dividers as their first stage [3], [6]. A low-power clock multiband divider for Bluetooth, Zigbee, and IEEE 802.15.4 and 802.11 a/b/g WLAN frequency synthesizers based on pulse-swallow topology is reported in [1], and it is implemented using a 0.18µm CMOS technology. The multiband divider consists of a wide band multimodulus 32/33/47/48 prescaler and swallow (S) counter and p-counter.

In the proposed system the E-TSPC 2/3 prescaler is replaced by the U-TSPC 2/3 prescaler [7].

II. BLOCK DIAGRAM

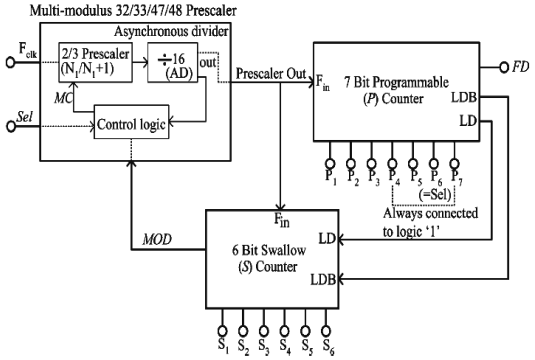

Fig.1. Existing Multiband Flexible Divider

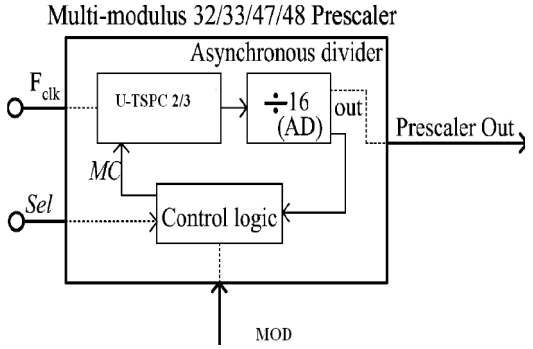

Fig.2. Proposed Multi-Modulus 32/33/47/48 Prescaler

In the existing system, a dynamic logic multiband flexible integer-N divider based on pulse-swallow topology[1] is proposed, which uses a low-power wide band 2/3 prescaler and a wide band multimodulus 32/33/47/48 prescaler as shown in Fig.1. The divider also uses an improved low-power loadable bit-cell for the Swallow S-counter.

III. U-TSPC 2/3 PRESCALER

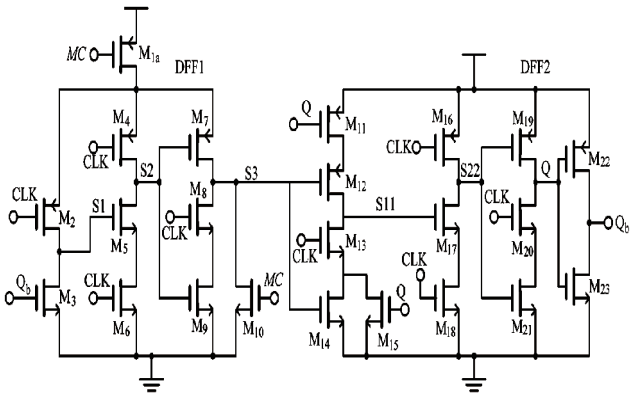

Fig.3. U-TSPC 2/3 Prescaler

In this section an ultra low power 2/3 prescaler is introduced from [7] as shown in Fig.3, and this is the further improved version of the Existing prescaler. An extra PMOS transistor M1a is connected between the power supply and flip-flop DFF1 whose input is the control logic signal MC. Ideally, DFF1 should not be active during the divide-by-2 mode as only DFF2 participates in the divide-by-2 operation. In this new design, when the control logic MC is logically high during the divide-by-2 mode, the PMOS transistor M1a is turned-off and DFF1 is disconnected from the power supply. Thus by switching off DFF1 completely during the divide-by 2 mode, the short circuit power and switching power of DFF1 is removed completely.

The divide-by-3 operation is performed when the control signal MC goes logically low during which the PMOS transistor M1a turns on and supplies power to

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Volume 4, Issue 1, ISSN (Online): 2249–071X, ISSN (Print): 2278–4209

DFF1. The divide-by-3 operation is performed same as existing design. In this design, DFF1 operates at a reduced supply voltage due to the Vds drop across transistor M1a. Since the frequency of operation is directly related to the power supply, the maximum operating frequency of Proposed Design becomes lower than that of the existing. The PMOS transistor M1 in existing design is removed in U-TSPC 2/3 prescaler, thus making the first stage of DFF1 similar to that of first stage in prescalers designed using E-TSPC flip-flops. With this modification, the maximum frequency of operation of the proposed U-TSPC 2/3 prescaler [7] is improved and is almost same as that of the existing.

The power consumed by this circuit in the divide-by-2 mode is given by the switching and short circuit power of DFF2 alone as in (1)

$$P_{2/3\_U-TSPC} = P_{switching-DFF2} + P_{short-DFF2}. \quad (1)$$

Power consumption of the ultra low power 2/3 prescaler is shown in the Fig.4.

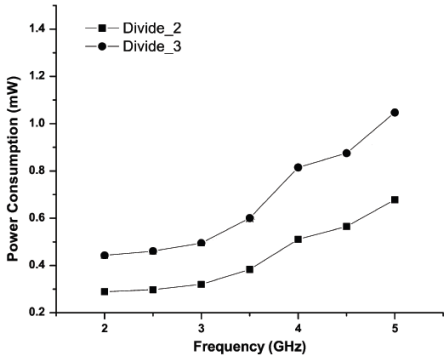

Fig.4. Measured Power Consumption of the Proposed Prescaler Units.

IV. 32/33/47/48 Prescaler Using Ultra Lowpower 2/3Prescaler

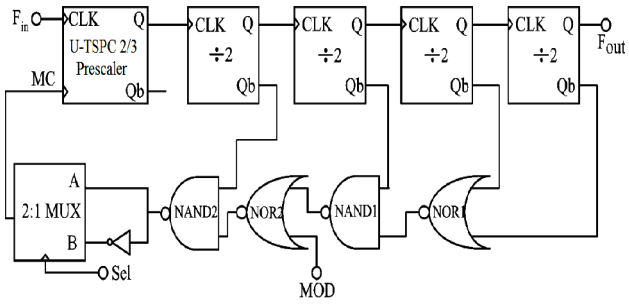

Fig.5. Multimodulus 32/33/47/48 Prescaler Using U-Tspc 2/3 Prescaler

The proposed wide band multimodulus prescaler is shown in Fig. 5, which can divide the input frequency by 32, 33, 47, and 48. It is similar to the 32/33 prescaler. But it consists of additional inverter and a multiplexer as like existing design. This prescaler performs additional divisions (divide- by-47 and divide-by-48) without any extra flip-flop, thus saving a considerable amount of power and also reducing the complexity of multiband divider which will be discussed below. The multimodulus prescaler consists of the ultra low power 2/3 ($N_1/(N_1+1)$) prescaler [7], four divide-by-2 circuits ((AD)=16) and combinational logic circuits for getting multiple division ratios. Beside the usual MOD signal for controlling N/(N+1)) divisions, the additional control signal Sel is used to switch the prescaler between 32/33 and 47/48 modes.

A. Case 1: Sel= '0'

When Sel = '0' , the output from the NAND2 gate is directly transferred to the input of 2/3 prescaler and the multimodulus prescaler operates as the normal 32/33 prescaler, where the division ratio is controlled by the logic signal MOD. If MC='1', the 2/3 prescaler operates in the divide-by-2 mode and when MC='0', the 2/3 prescaler operates in the divide-by-3 mode. If MOD = '1', the NAND2 gate output switches to logic "1" (MC = '1') and the wide band prescaler operates in the divide- by-2 mode for entire operation. The division ratio N of the multimodulus prescaler is

$$N= (AD*N_1) + (0* (N_1 + 1)) = 32. \quad (2)$$

Where N_1 ='2' and AD = '16' is fixed for the entire design. If MOD = '0' , for 30 input clock cycles 'MC' remains at logic "1", where wideband prescaler operates in divide-by-2 mode and, for three input clock cycles, 'MC' remains at logic "0" where the wideband prescaler operates in the divide-by-3 mode. The division ratio N+1 of the multimodulus prescaler is

$$N+1 = ((AD - 1) * N_1) + (1 * (N_1 +1)) = 33. \quad (3)$$

B. Case 2: Sel = '1'

When Sel = '1', the inverted output of the NAND2 gate is directly send to the input of 2/3 prescaler and the multimodulus prescaler operates as a 47/48 prescaler, and the division ratio is controlled by the signal 'MOD'. If MC='1', the 2/3 prescaler operates in divide-by-3 mode and when MC='0', the 2/3 prescaler operates in divide-by-2 mode'. If MOD='1', the division ratio N +1 performed by the multimodulus prescaler is same as (6) except that the wide band prescaler operates in the divide-by-3 mode for the entire operation given by

$$N +1 = (AD * (N_1 + 1)) + (0 * N_1) = 48 \quad (4)$$

If MOD = '1', the division ratio N performed by the multimodulus prescaler is

$$N = ((AD - 1) * (N_{1+1})) + (1 * N_1) = 47 \quad (5)$$

C. A 32/33 Prescaler Using U-TSPC 2/3 Prescaler

The amount of power saved by this prescaler in divide-by-2 mode is ideally 67% compared to that of existing prescaler and also reduces power consumption by 50% compared to other prescaler during divide-by-3 operation. The assumption here is, during the divide-by-2 operation no power is consumed by DFF1 neglecting the leakage current. To further verify the advantages of the proposed ultra low power prescaler , a divide 32/33 dual modulus unit is implemented with the ultra low power 2/3 prescaler as shown in Fig.5.additionally 47/48 also performed with additional 2:1 multiplexer and a not gate[1]. In this 32/33/47/48 prescaler, the proposed 2/3 prescaler unit is followed by four stages of the toggled TSPC divide- by-2 units.

When the signal MOD is logically high, the 32/33 prescaler function as divide-by-32 unit and the control logic signal MC to the 2/3 prescaler goes logically high

allowing it to operate in divide-by-2 mode for the whole 32 clock cycles. Since control logic signal MC is logically high, DFF1 in the ultra low power 2/3 prescaler is completely turned-off for the entire 32 input clock cycles. When control logic signal MOD is logically low, the 32/33 prescaler unit function as divide-by-33 unit during which 2/3 prescaler operates in divide-by-3 mode for 3 input clock cycles and in divide-by-2 mode for 30 input clock cycles during which DFF1 in the ultra low power 2/3 prescaler turns off completely thus reducing the power consumption of 32/33 prescaler using ultra low power 2/3 prescaler.

D. Power Saving Analysis During Divide-by-32 Mode

The total power consumed by the 32/33 prescaler using existing 2/3 prescaler during divide-by-32 is equal to the sum of switching and short circuit power of the DFF1, DFF2 over 32 clock cycles, power consumed by four asynchronous divide-by-2 circuits, and the power consumed by the logic gates

$$P_{32\_Exixsting} = P_{switching\ -DFF1} + P_{switching\ -DFF2} + P_{div-By-16} + P_{short\ -\ DFF2} + P_{short-S3-DFF1} + P_{logic\ Ic\_Gates}. \quad (6)$$

The power consumed by the four asynchronous divide-by-2 circuits is given by (7)

$$P_{Div-by-16} = \frac{\sum_{i=1}^{4} f_P C_{Li} V_{dd}^2}{2^{i=1}} \sum_{i=1}^{4} I_{SCi} V_{dd} \quad (7)$$

Here, f_P is the output signal frequency from the 2/3 prescaler which can be half or one-third of the input clock signal and I_{SCi} is the total short-circuit current of the each divide-by-2 circuit. Each of the asynchronous divider toggles at half the operating frequency of the preceding divide-by-2 circuit. Similarly, the power consumed by the 32/33 prescaler during the divide-by-32 operation using the ultra low power 2/3 prescaler is equal to the sum of switching and short circuit power of DFF2 over 32 clock cycles (DFF1 off) and the power consumed by the 4 asynchronous dividers and logic gates as given by (8). Here, the power consumed by the 4 asynchronous dividers is the same as in (7)

$$P_{32\_Existing} = P_{Switching-DFF2} + P_{short-DFF2} + P_{Div-by-16} + P_{logic\ ic\_gates} \quad (8)$$

Here, the power consumed by DFF2 is the same in existing 2/3 prescaler and ultra low power 2/3 prescaler. The power saved by the 32/33 prescaler during the divide-by-32 mode using ultra low power 2/3 prescaler is obtained from (6) and (8), which is equal to the power consumed by DFF1 of the Design-I prescaler. Here, the power consumed by DFF1 always refers to the Design-I 2/3 prescaler since power consumed by DFF1 of Design-II prescaler is zero

$$P_{32\_saved} = P_{short-s3-DFF1} + P_{switching-DFF1} \quad (9)$$

E. Power Saving Analysis During Divide-by-33 Operation

The total power consumed by the exixting 32/33 prescaler during the divide-by-33 operation is equal to the sum of switching power of the flip-flops DFF1, DFF2, short circuit power of DFF2, short circuit in the 3rd stage of DFF1 over 30 clock cycles, short circuit and switching power of DFF1, DFF2 over 3 clock cycles, power consumed by four asynchronous divide-by-2 circuits and the power consumed by the digital gates.

$$P_{33\_Existing} = \frac{30}{33}\left(P_{Switching-DFF1} + P_{short-S3-DFF1} + P_{short-DFF2} + P_{switching-DFF2}\right) + P_{Div-by-16} + \frac{3}{33}\left(P_{switching-DFF1} + P_{switching-DFF2} + P_{short-DFF1} + P_{short-DFF2}\right) + P_{logic\ ic_{gates}} \quad (10)$$

Similarly, the power consumed by the 32/33 prescaler using ultra low power 2/3 prescaler during the divide-by-33 operation is equal to the sum of the switching, short circuit power of DFF2 over 30 clock cycles, switching and short circuit power of DFF1, DFF2 over 3 clock cycles, power consumed by the 4 asynchronous dividers and digital logic gates given by (11)

$$P_{33\_U-TSPC} = \frac{30}{33}\left(P_{Switching-DFF2} + P_{short-DFF2}\right) + P_{Div-by-16} + \frac{3}{33}\left(P_{switching-DFF1} + P_{switching-DFF2} + P_{short-DFF1} + P_{short-DFF2}\right) + P_{logic\ ic\_gates}. \quad (11)$$

Since power consumed by DFF2, 4 asynchronous divide-by-2 dividers and the logic gates are same in both cases, the total amount of power saved by the 32/33 prescaler during the divide-by-33 using ultra low power 2/3 prescaler is equal to 0.9 times the power consumed during divide-by-32. From the analysis discussed above, it is verified that existing prescaler reduces power by almost 50% during the divide-by-3 operation but consumes the same power as conventional TSPC 2/3 prescaler does during the divide-by-2 operation. The proposed ultra low power 2/3 prescaler consumes same power as the existing prescaler does during the divide-by-3 operation but saves 67% of power during the divide-by-2 operation which is also theoretically verified in the design of 32/33 prescaler[7].

Here the design is not optimized and devices of the same size (3µm for PMOS and 2µm for NMOS) is employed for all the flip-flops in the asynchronous divide-by-2 stages. The simulation results shows that 32/33 prescaler consumes a power of 788 µW, 807 µW during divide-by-32, divide-by-33 modes respectively at 2.5 GHz. The asynchronous dividers and logic gates account for 60% of total power consumption of the 32/33 prescaler. By progressively reducing the device width ratio of PMOS/NMOS of stage 1 to stage 4 in the asynchronous divide-by-2 circuits as follows: 3 µm/2 µm, 2.25 µm/1.5 µm, 1.5 µm/1µ m, 0.75 µm/0.5µ m, according to the decreasing operating frequency of the flip-flops, the power consumption can be further reduced.

The simulations shows that the asynchronous stage and logic gates account for about 56% of total power consumption and the total power consumption of the 32/33 prescaler is reduced to 713 µW, 730 µW during divide-by-32 and divide-by-33 operating modes respectively. Further attempts to reduce the transistor widths below 0.75 m for PMOS and 0.5 m NMOS affect the functioning of the prescaler. The experimental results for the 32/33 prescaler are not optimized but the functioning of the proposed 2/3 prescaler is verified in the design of 32/33 prescaler.

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V. MULTIBAND FLEXIBLE DIVIDER

The single-phase clock multiband flexible divider which is shown in Fig.1 [1], consists of the multimodulus 32/33/47/48 prescaler, a 7-bit programmable P-counter and a 6-bit swallow S-counter. The multimodulus 32/33/47/48 prescaler is briefly discussed in Section IV. The control signal Sel decides whether the divider is operating in lower frequency band or higher band.

A. Swallow (s) Counter

The 6-bit S-counter is shown in Fig.6, which consists of six asynchronous loadable bit-cells, a NOR-embedded DFF and additional logic gates were allowing it to be programmable from 0 to 31 for low-frequency band and from 0 to 47 for the high-frequency band [1]. The asynchronous bit-cell used in this counter is shown in Fig.7, and it is similar to the bit-cell reported in [8], except it uses two additional transistors M_6 and M_7 whose inputs are controlled by the logic signal MOD. If MOD signal is logically high, nodes S1 and S2 switch to logic "0" and the bit-cell does not perform any function. The MOD signal goes logically high only when the S-counter finishes counting down to zero. If MOD and LD are logically low, the bit-cell acts as a divide-by-2 unit. If MOD is logically low and LD is logically high, the input bit PI is transferred to the output.

In the initial state, MOD = '0', the multimodulus prescaler selects the divide-by-(N+1) mode (divide-by-33 or divide-by-48) and P, S counters start down counting the input clock cycles. When the S-counter finishes counting, (MOD) switches to logic "1" and the prescaler changes to the divide-by-N mode (divide-by-32 or divide-47) for the remaining (P-S)clock cycles. During this mode, since S-counter is idle, transistors M_6 and M_7 which are controlled by MOD, keep the nodes S1 and S2 at logic "0," thus saving the switching power in S-counter for a period of (N * (P-S)) clock cycles. Here, the programmable input (PI) is used to load the counter to a specified value from 0 to 31 for the lower band and 0 to 48 for the higher band of operation.

B. Programmable (P) Counter

The programmable P-counter is a 7-bit asynchronous down counter which consists of 7 loadable bit-cells [8] and additional logic gates. Here, bit P_7 is tied to the Sel signal of the multimodulus prescaler and bits P_4 and P_7 are always at logic "1." The remaining bits can be externally programmed from 75 to 78 for the lower frequency band and from 105 to 122 for the upper frequency band.

When the p-counter finishes counting down to zero, LD switches to logic "1" during which the output of all the bit-cells in S-counter switches to logic "1" and output of the NOR embedded DFF switches to logic "0" (MOD = '0') where the programmable divider get reset to its initial state and thus a fixed division ratio is achieved. If a fixed 32/33(N/(N + 1)) dual-modulus prescaler is used, a 7-bit P-counter is needed for the low-frequency band (2.4 GHz) while an 8-bit P-counter would be needed for the high-frequency band (5–5.825 GHz) with a fixed 5-bit S-counter. Thus, the multimodulus 32/33/47/48 prescaler eases the design complexity of the P-counter.

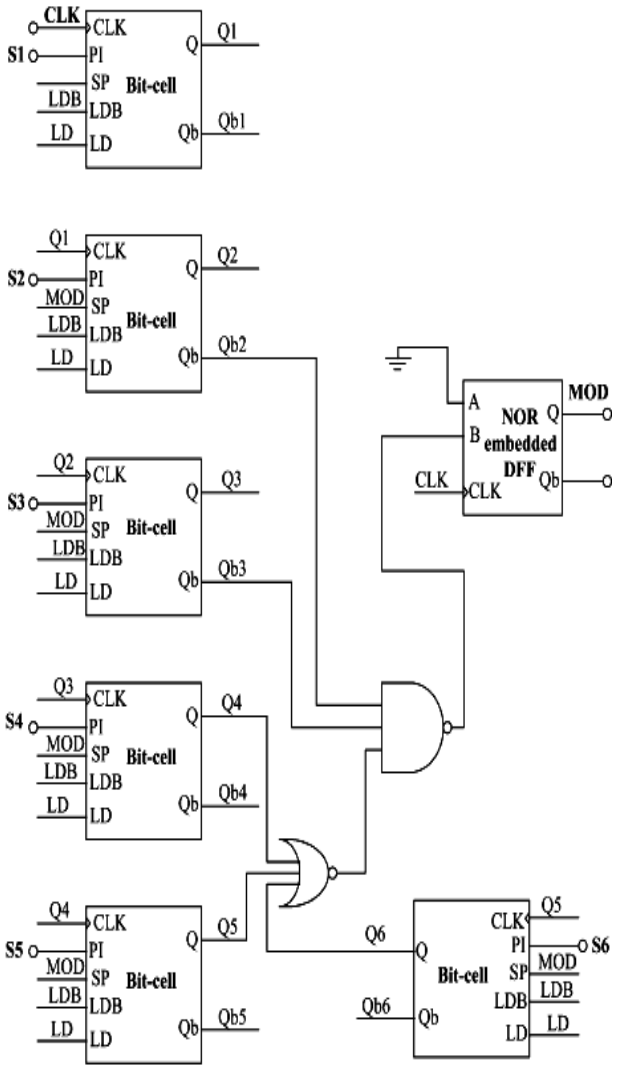

Fig.6. Swallow (s) Counter

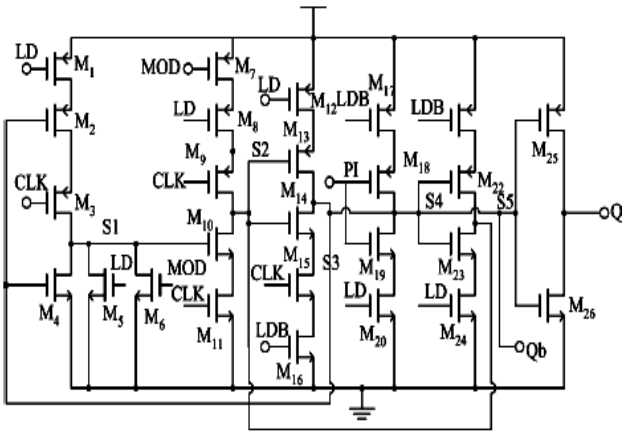

Fig.7. Asynchronous loadable bit-cell for S-counter.

VI. SIMULATIONS

From the simulation results, the wide band 2/3 prescaler has the maximum operating frequency of 8 GHz with a power consumption of 0.92 and 1.73 mW during the divide-by-2 and divide-by-3 modes, respectively. The proposed multimodulus prescaler has the maximum

operating frequency of 7.2 GHz (simulation) with a power consumption of 1.52, 1.60, 2.10, and 2.13 mW during the divide-by-32, divide-by-33, divide-by-47 and divide-by-48, respectively.

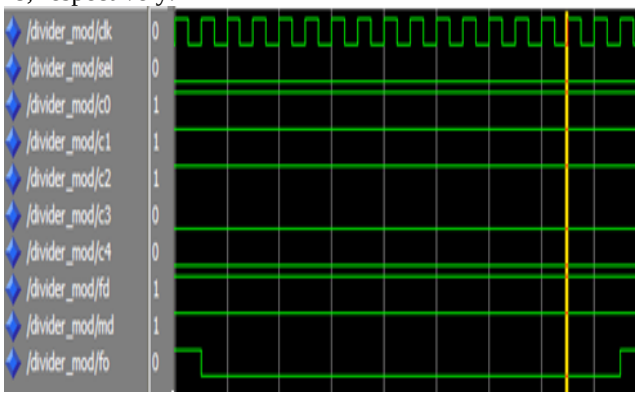

Fig.8. Simulation Result of U-TSPC 2/3 Prescaler

The simulation waveform of the proposed 2/3 prescaler is shown in the Fig.8. Fig.9 shows the overall simulation of this proposed system. The total equivalent gate count of the Existing multimodulus prescaler circuit[1] is 262, and this equivalent gate count is reduced upto 221 in the proposed system.

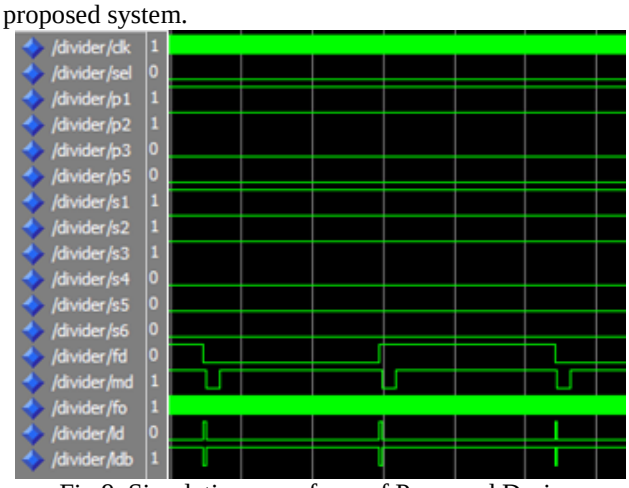

Fig.9. Simulation waveform of Proposed Design

VII. Conclusion

In this paper, an ultra low power 2/3 prescaler is used in wide band multimodulus 32/33/47/48 prescaler. A dynamic logic multiband flexible integer-N divider is designed which uses the ultra low power 2/3 prescaler [7]. The values of P- and S-counters can actually be programmed to divide over the whole range of frequencies from 1 to 6.2 GHz with finest resolution of 1 MHz and variable channel spacing. since interest lies in the 2.4- and 5–5.825-GHz bands of operation, the P- and S-counters are programmed accordingly. The proposed multiband flexible divider also uses an improved loadable bit-cell for Swallow S-counter and consumes a power of 0.96 and 2.2 mW in 2.4- and 5-GHz bands.

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